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EXAMINER	
TSAI, HENRY	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/608,624	Applicant(s) JOURDAN ET AL.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/8/04* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-20 and 22-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-7* is/are allowed.

6)☒ Claim(s) *1-3,9-16,20 and 22-37* is/are rejected.

7)☒ Claim(s) *17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-3, 9-15, 20, 22, and 28-32 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims recite nothing more than a nonstatutory subject matter.

Claims to computer-related inventions that are clearly nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely natural phenomena such as magnetism, and abstract ideas or laws of nature which constitute "descriptive material. "Abstract ideas, Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759, or the mere manipulation of abstract ideas, Schrader, 22 F.3d at 292-93, 30 USPQ2d at 1457-58, are not patentable. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data (See MPEP section 2106, IV, B, 1).

The examiner submits that the claims are

1) not tangibly embodied on a computer readable medium; and

2) non-functional descriptive material; data *per se* is non-statutory-- this claim fails to recite the necessary functional interrelationship within the architecture to constitute a data structure.

As to claims 1-3, in claim 1, line 1, "a memory entry" is not a hardware element. It is only a unit (an abstract term, such as one inch is a unit for a length) for a memory size. Further, "to store a trace" is just an intended use and in claim 1, line 2, "having a multi-entry, single exit architecture" is just an alternate trace architecture. Therefore, non-functional descriptive material exists in the claimed invention. Claims 1-3 are directed to non-statutory subject matter. Same problems exist in Claims 20, and 22 (same as claims 31, and 32).

As to claims 9-15, in claim 9, lines 2-5, the method steps of "predicting an address"; "determining whether the predicted address matches an address of a terminal instruction"; and "selecting one of the extended block in the event of a match" all can be mental steps. Again, non-functional descriptive material exists in the claimed invention. Therefore, they are directed to non-statutory subject matter.

As to claims 28 and 29, line 1, "a trace" and "a sequence of program instruction" are not a hardware element. Therefore,

non-functional descriptive material exists in the claimed invention.

As to claim 30, line 1, as set forth, "a memory entry" is not a hardware element. It is only a unit (an abstract term, such as one inch is a unit for a length) for a memory size. Further, "stored in a memory" is just an intended use.

Claim Objections

3. Claims 31-37 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 20, 22, 23-27 respectively. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

4. Claims 22 and 32 are objected to because of the following informalities:

in claim 22, line 1, "trace" should read -apparatus- since a trace is not the claimed invention of claim 20; and

in claim 32, line 1, "trace" should read -apparatus- since a trace is not the claimed invention of claim 32.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-3, 20, 22, and 28-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 1, as set forth above, "a memory entry" is not a hardware element. It is only a unit (an abstract term, such as one inch is a unit for a length) for a memory size. Therefore, non-functional descriptive material exists in the claimed invention. The real claimed invention is unclear. Similar problems exist in claims 20 and 31.

In claim 28, line 1, "trace" and "a sequence of program instruction" are not a hardware element. The real claimed invention is unclear.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-3, 16, 20, 22, and 28-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Agarwal (U.S. Patent No. 5,966,541), hereinafter referred to as Agarwal'541.

Referring to claim 1, Agarwal'541 discloses as claimed: a memory entry (the space containing blocks 101, 102 and 103 as shown in Fig. 8; Note a memory entry is best broadly and reasonable interpreted a space where information can be stored and retrieved), storing a trace (including blocks 101, 102 and 103 as shown in Fig. 8) having a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture. Note Fig. 8 is best reasonably and broadly interpreted to comprise many traces such as from block 101 to block 103 and from block 102 to block 103 as shown in Fig. 8.

Referring to claim 16, Agarwal'541 discloses as claimed: A processing engine (inherently existing in Agarwal'541's system), comprising: a front end stage to store blocks (in memory 703, see Fig. 11, and Col. 11, line 36), including blocks 101, 102 and 103 as shown in Fig. 8) of instructions in a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture when considered according to program flow, and an execution unit (inherently existing in Agarwal's system) in communication with the front end stage.

Referring to claims 20 and 31, Agarwal'541 discloses as claimed: apparatus, comprising a memory entry to store (in memory 703, see Fig. 11, and Col. 11, line 36) a sequence of program

instructions (from I3 to I9 see Fig. 8) as a trace (including blocks 101, 102 and 103 as shown in Fig. 8), the instructions defining a program flow that progresses (note Fig. 8 shows the program flow progresses instruction to instruction) from any instruction (instructions from I3 to I8 see Fig. 8) therein to a last instruction (last instruction I9 see Fig. 8) in the trace and in which the trace has multiple separate prefixes (block 101 and block 102 are the prefixes as shown in Fig. 8).

Referring to claim 28, Agarwal'541 discloses as claimed: a trace (including blocks 101, 102 and 103 as shown in Fig. 8), comprising a sequence of program instructions (from I3 to I9 see Fig. 8) stored together (in memory 703, see Fig. 11, and col. 11, line 36) assembled in order according to program flow, the sequence having a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture. Note as set forth above, Fig. 8 is best reasonably and broadly interpreted to comprise many traces such as from block 101 to block 103 and from block 102 to block 103 as shown in Fig. 8.

As to claims 2 and 29, Agarwal'541 also discloses: the trace being a complex trace (including blocks 101, 102 and 103 as shown in Fig. 8) having multiple independent prefixes (block 101 and

block 102 as shown in Fig. 8) and a common, shared suffix (block 103 is the as shown in Fig. 8).

As to claims 3, 22, 30, and 32, Agarwal'541 also discloses: the entry (including such as blocks 101, 102 and 103 as shown in Fig. 8) being indexed by an address of a terminal instruction therein. Note, inherently, the Agarwal's entry is indexed by an address of a terminal instruction (such as I3 for block 101, I5 for block 102 and I8 for block 103) therein. Note a terminal instruction is best reasonably and broadly interpreted to be at the either end of the block, such as I5 and I7 are the terminal instruction of block 102 as shown in Fig. 8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 23-27, and 33-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over (U.S. Patent No. 5,966,541) (Hereinafter referred to as Agarwal'541).

Agarwal'541 discloses the claimed invention except for: comprising a memory comprising storage for a plurality of traces and means for indexing the traces by an address of a last instruction therein according to program flow (claims 23 and 33).

However, as set forth above, Agarwal'541 discloses: the entry (including such as blocks 101, 102 and 103 as shown in Fig. 8) being indexed by an address of a terminal instruction therein. Note, inherently, the Agarwal's entry is indexed by an address of a terminal instruction (such as I3 for block 101, I5 for block 102 and I8 for block 103) therein. Note a terminal instruction is best reasonably and broadly interpreted to be at the either end of the block, such as I5 and I7 are the terminal instruction of block 102 as shown in Fig. 8.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Agarwal's machine to comprise a memory comprising storage for a plurality of traces and means for indexing the traces by an address of a last instruction therein according to program flow since it is the alternative arrangement for indexing the traces as comparing with that of Agarwal's system.

As to claims 24 and 34, Agarwal'541 also discloses traces (such as that including blocks 101, 102 and 103 as shown in Fig. 8) including a plurality of instructions (I3-I9, see Fig. 8) assembled according to program flow (see Fig. 8).

As to claims 25 and 35, Agarwal'541 also discloses as claimed: a memory (the space containing blocks 101, 102 and 103 as shown in Fig. 8; Note a memory is best broadly and reasonable interpreted a space where information can be stored and retrieved), wherein at least one trace (including blocks 101, 102 and 103 as shown in Fig. 8) having a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture. Note Fig. 8 is best reasonably and broadly interpreted to contain many traces such as from block 101 to block 103 and from block 102 to block 103 as shown in Fig. 8.

As to claims 26 and 36, Agarwal'541 also discloses: at least one trace (including blocks 101, 102 and 103 as shown in Fig. 8) having separate prefixes (block 101 and block 102 as shown in Fig. 8) and a common suffix (block 103 as shown in Fig. 8).

As to claims 27 and 37, Agarwal'541 also discloses: at least one trace including at least three segments (including blocks 101, 102 and 103 as shown in Fig. 8) of executable

instructions in which, when considered according to program flow, first and second segments (blocks 101, and 102 as shown in Fig. 8) are mutually exclusive of each other and lead into the third segment (block 103 as shown in Fig. 8).

Allowable Subject Matters

9. Claims 4-7 are allowed.

10. Claims 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: Agarwal, the closest references, do not teach or fairly suggest:

a front-end system comprising: the extended block cache system having a block predictor to store masks associated with the complex traces, the masks distinguishing the prefixes from each other (in claim 4);

Response to Arguments

12. Applicant's arguments filed 4/8/04 have been fully considered but they are not deemed to be persuasive.

Regarding the 35 U.S.C. §112, second paragraph problems, Applicant's response has not completely overcome these rejections.

Regarding the 101 rejection under 35 U.S.C. 101, Applicants argue that "Claim 1, for example, recites storage of a trace which has a multiple-entry, single exit architecture. Claim 20 recites a trace that defines program flow that progresses from any instruction therein to a last instruction in the entry. Claim 20 also recites a trace that has multiple prefixes" (at page 8, lines 7-10). Examiner disagrees with Applicants. As set forth above, as to claims 1-3, in claim 1, line 1, "a memory entry" is not a hardware element. It is only a unit (an abstract term, such as one inch is a unit for a length) for a memory size. Further, "to store a trace" is just an intended use and in claim 1, line 2, "having a multi-entry, single exit architecture" is just an alternate trace architecture. Therefore, non-functional descriptive material exists in the claimed invention. Claims 1-3 are directed to non-statutory

subject matter. Same problems exist in Claims 20, 22, 31, and 32.

Applicants also argue that "Agarwal does not describe any relationship between the program flow and memory. Agarwal does not explain which portions of this program flow are stored in a common entry or, for example, which portions might be stored across multiple entries" **(at page 9, lines 11-14)**; and "**There is absolutely no disclosure to suggest that blocks 101-103 are stored in a common memory entry as recited in this claim. Claim** 2 also distinguishes over this reference" **(at page 9, lines 19-20).** Examiner disagrees with Applicants. Agarwal'541 does disclose portions of this program flow are stored in a common memory entry in memory 703, see Fig. 11, and Col. 11, line 36. The common memory entry includes blocks 101, 102 and 103 as shown in Fig. 8 and multiple entries, from I2 to I3 and from I2 to I5, are also shown in Fig. 8.

Applicants also argue that "**Claim 3 recites that the entry is indexed by an address of a terminal instruction therein.** Agarwal does not disclose this subject matter"(at page 9, last paragraph); and "**Claim 22 recites: wherein the memory entry is indexed by an address of a terminal instruction therein. Agarwal discloses no such subject matter and does not render it** inherent" **(at page 10, lines 24-25).** Examiner disagrees with

Applicants. As set forth in the art rejections above, Agarwal'541 also discloses: the entry (including such as blocks 101, 102 and 103 as shown in Fig. 8) being indexed by an address of a terminal instruction therein. Note, inherently, the Agarwal's entry is indexed by an address of a terminal instruction (such as I3 for block 101, I5 for block 102 and I8 for block 103) therein. A terminal instruction is best reasonably and broadly interpreted to be at the either end of the block, such as I5 and I7 are the terminal instruction of block 102 as shown in Fig. 8. This is consistent with that Applicant mentioned at page 9, last two lines:
"Agarwal's system also could index the instructions by the address of the first instruction in his blocks, not the terminal instruction".

Regarding claim 20, Applicants also argue that "Agarwal discloses only abstract blocks, each of which has a single-entry, single-exit structure. None of his blocks contains multiple separate prefixes" (at page 10, lines 18-19). Examiner disagrees with Applicants. As set forth above in the art rejections, Agarwal'541 discloses a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8) and the trace has multiple separate prefixes (block 101 and block 102 are the prefixes as shown in Fig. 8).

In summary, Agarwal teaches the claimed invention.

Contact Information

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

14. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account.

Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

June 1, 2004